AMENDMENTS TO THE CLAIMS:

Claim listing:

1-12. (Canceled)

13. (New) In a memory redundancy circuit in a memory module having a designated group of memory cells assigned to represent a logical portion of the memory structure and a redundant group of memory cells, the method comprising assigning the redundant group to the logical portion of the memory structure, responsive to a preselected designated group condition.

14. (New) The method of Claim 13, wherein the assigning comprises shifting data to the redundant group of memory cells responsive to a signal representative of the preselected designated group condition.

15. (New) The method of Claim 13, wherein the memory module further comprises a plurality of selectable switches, the plurality of selectable switches encoding the preselected designated group condition.

16. (New) The method of Claim 15, wherein the plurality of selectable switches comprises fuses.

17. (New) The method of Claim 15, wherein the preselected designated group condition comprises a "FAILED" condition, representative of a designated malfunction.

18. (New) The method of Claim 13, wherein each of the designated group of memory cells and the redundant group of memory cells comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

19. (New) In a memory circuit including pairs of designated memory cells and pairs of redundant memory cells, a method comprising redirecting a signal path from the designated memory cells to the redundant memory cells based on a failure of the designated memory cells.

20. (New) The method of claim 19 wherein the redirecting comprises shifting data to at least a portion of the redundant memory cells responsive to a signal representative of a preselected designated condition of at least a portion of the designated memory cells.

21. (New) The method of claim 20, wherein the memory circuit further comprises a plurality of selectable switches, the plurality of selectable switches encoding an encoded signal and having a logarithmic relationship to the number of pairs of designated memory cells.

22. (New) The method of Claim 21, wherein the plurality of selectable switches comprises fuses.

23. (New) The method of Claim 19, wherein the designated memory cells and the redundant memory cells each comprises one of a row pair of memory cells and a column pair of memory cells.

24. (New) The method of Claim 19, wherein the designated memory cells and the redundant memory cells each comprises a line pair of memory cells.

25. (New) In a memory circuit including designated memory cells, redundant memory cells and a controller, a method comprising redirecting a signal path from the designated memory cells to the redundant memory cells based on a failure of at least a portion of the designated memory cells, the controller comprising a plurality of

selectable switches having a logarithmic relationship to the number of designated memory cells.

26. (New) The method of claim 25 wherein the redirecting comprises shifting data to at least a portion of the redundant group of memory cells responsive to a signal representative of the failure of at least a portion of the designated memory cells.

27. (New) The method of Claim 25, wherein the plurality of selectable switches comprises fuses.

28. (New) The method of Claim 25, wherein the designated memory cells and the redundant memory cells each comprises one of a row pair of memory cells and a column pair of memory cells.

29. (New) The method of Claim 25, wherein the designated memory cells and the redundant memory cells each comprises a line pair of memory cells.